

8. The solid-state imaging apparatus according to claim 1, wherein

the third semiconductor region extends into the first semiconductor region largely than the extending of the second semiconductor region into the first semiconductor region.

9. The solid-state imaging apparatus according to claim 1, wherein

the third semiconductor region has an impurity concentration higher than an impurity concentration of the fourth semiconductor region.

10. The solid-state imaging apparatus according to claim 1, wherein

an impurity concentration of a region between the third and fourth semiconductor regions is lower than an impurity concentration of the fourth semiconductor region.

11. The solid-state imaging apparatus according to claim 1, further comprising

a second voltage supply portion, provided separately from the first voltage supply portion, for supplying a reference voltage to the fourth semiconductor region arranged in the pixel region,

the second voltage supply portion includes a sixth semiconductor region of the second conductivity type, and a second electrode connected to the sixth semiconductor region, and

a power source for supplying the voltage to the first electrode is separately provided from a power source for supplying the voltage to the second electrode.

12. The solid-state imaging apparatus according to claim 1, further comprising

a transfer MOS transistor transferring a carrier from the first semiconductor region to the second semiconductor region, and

the transfer MOS transistor is buried channel type.

13. A solid-state imaging apparatus having a semiconductor substrate of a first conductivity type, and a plurality of pixels arranged in a pixel region of the semiconductor substrate, each pixel including a photoelectric conversion region, an amplifying transistor for amplifying a signal based on a signal carrier generated in the photoelectric conversion region and for outputting an amplified signal and a floating diffusion region of the first conductivity type connected to a gate of the amplifying transistor, such that a potential of the semiconductor substrate is controlled to perform an electronic shutter operation, wherein the pixel region includes:

a first semiconductor region of the first conductivity type for forming a part of the photoelectric conversion region;

a second semiconductor region of the first conductivity type, formed separately from the first semiconductor region, for accumulating the carrier generated in the first semiconductor region;

a third semiconductor region of a second conductivity type arranged under the second semiconductor region, for operating as a potential barrier holding the accumulated carrier in the second semiconductor region;

a fourth semiconductor region of the second conductivity type extending between the first semiconductor region and the semiconductor substrate, and between the third semiconductor region and the semiconductor substrate; and

a first voltage supply portion for supplying a reference voltage to the third semiconductor region, the first voltage supply portion includes a fifth semiconductor region of the second conductivity type arranged in the pixel region, and a first electrode connected to the fifth semiconductor region,

a plurality of the first voltage supply portions are arranged in the pixel region,

the fifth semiconductor region is arranged in an active region adjacent to an active region in which the second semiconductor region, floating diffusion region or the amplifying transistor is arranged, and an isolation region is sandwiched between the active region in which the fifth semiconductor region is arranged and the active region in which the second semiconductor region, floating diffusion region or the amplifying transistor is arranged,

the third semiconductor region extends into the first semiconductor region largely than the extending of the second semiconductor region into the first semiconductor region,

the third semiconductor region has an impurity concentration higher than an impurity concentration of the fourth semiconductor region,

an impurity concentration of a region between the third and fourth semiconductor regions is lower than an impurity concentration of the fourth semiconductor region,

a transfer MOS transistor transferring a carrier from the first semiconductor region to the second semiconductor region is provided, and

the transfer MOS transistor is buried channel type.

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